A 6-bit 2GS/s CMOS Time-Interleaved ADC for Analysis of Mixed-Signal Calibration Techniques

Benjamín T. Reyes ‡, Lucas Tealdi†, German Paulina†,
Emanuel Labat†, Raúl Sanchez†, Pablo S. Mandolesi*, and Mario R. Hueda‡

‡ Laboratorio de Comunicaciones Digitales - Universidad Nacional de Córdoba - CONICET
Av. Vélez Sarsfield 1611 - Córdoba (X5016GCA) - Argentina
† Fundación Fulgor - Romagosa 518 - Córdoba (5000) - Argentina
* GISEE - LMNE - Universidad Nacional del Sur - Av. Alem 1253 - Bahía Blanca - Argentina
Emails: {breyes, mhueda}@efn.uncor.edu

***Abstract*— A 6-bit 2-GS/s time interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC) is designed and fabricated in a 0.13 μm CMOS process. The architecture uses 8 time-interleaved track-and-hold amplifiers (THA), and 16 SAR ADC's. The chip includes (*i*) a programmable delay cell array to adjust the interleaved sampling phase, and (*ii*) a 12 Gbps low voltage differential signaling (LVDS) interface. These blocks make the fabricated ADC an excellent platform to evaluate mixed-signal calibration techniques, which are of great interest for application in high-speed optical systems. Measurements of the fabricated ADC show 33.9 dB of peak signal-to-noise-and-distortion ratio (SNDR) and 192 mW of power consumption at 1.2 V.**

I. Introduction

Time-interleaved analog-to-digital converters (TI-ADC) are widely used to provide high-sampling rate for digital receivers architectures (e.g., wireline and optical links) [1]. A basic TI-ADC architecture includes M single converters (or channels) operating in a parallel fashion at frequency $1/T$ but with different sampling phases in order to achieve an overall sampling rate of M/T. It is well known that TI-ADC's are sensitive to mismatches of the offset, gain, and sampling phase among the channels. These impairments are collectively known as *fixed-pattern noise* (FPN).

Numerous calibration techniques for FPN compensation have been proposed [2]–[6]. Recently, *mixed-signal calibration* techniques have received special attention for applications in ultra-high speed optical communication systems [4], [5], [7]. For example, the minimization of the *mean squared error* (MSE) or the *bit-error rate* (BER) by using a gradient algorithm has been proposed in [8]. Typically, long computer simulation run time is required to evaluate the performance of mixed-signal calibration algorithms such as the one described in [8]. We highlight that this problem is exacerbated when the communication system under analysis includes complex algorithms such as powerful *forward error correction* (FEC) codes. In this context, emulation based on field-programmable gate array (FPGA) platforms are usually adopted to save time. From the above, it can be inferred that the design and fabrication of an integrated high-speed TI-ADC that includes (*i*) capabilities to adjust the sampling phase among the channels and (*ii*) a multigigabit interface to connect with powerful FPGA platforms is of great interest to design mixed-signal calibration algorithms for next-generation optical networks.

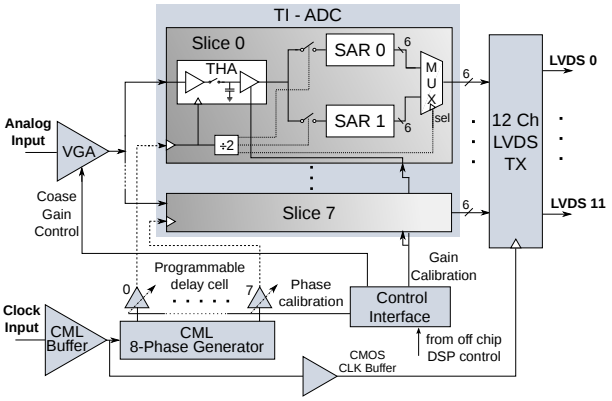

Fig. 1. Time-Interleaved ADC chip architecture.

This paper presents a 6-bit 2-GS/s time-interleaved *successive approximation register* (SAR) ADC. The architecture uses 8 time-interleaved track-and-hold amplifiers (THA), and 16 SAR ADC's. The chip includes (*i*) a programmable delay cell array to adjust the interleaved sampling phase, and (*ii*) a 12 Gbps low voltage differential signaling (LVDS) interface. The designed ADC can be used to save time during the design of mixed-signal calibration techniques [8]. The ADC fabricated in a 0.13μm CMOS process achieves 33.9 dB of signal-to-noise-and-distortion ratio (SNDR) and 192 mW of power consumption at 1.2 V.

The rest of this paper is organized as follows. Section II describes the chip architecture. Section III presents the design of the asynchronous SAR ADC and details of the comparator offset calibration circuit. Section IV shows results from measurements of the fabricated ADC. Finally, concluding remarks are drawn in Section V.

II. Architecture of the TI-ADC

The chip architecture is shown in Fig. 1. Next we present the design requirements and details of the architecture of the fabricated TI-ADC.

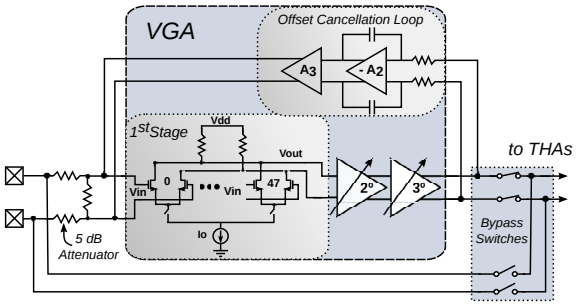

Fig. 2. Variable gain amplifier (VGA) composed by a 3-stage differential amplifier with digital gain control.

A. Requirements

This ADC is required to be the core of a test/verification platform for time skew mismatch calibration algorithms in time interleaved ADCs. Towards this end, the design includes eight interleaved THA and sixteen single SAR converters to achieve an overall high sampling rate such as 2 GHz. The main requirement from the point of view of the algorithm verification concept is a wide flexibility of clock phase control in each THA. The sampling frequency of the TI-ADC can be set from 200 MHz to 2 GHz. Furthermore, the chip has to be able to vary around a $\pm 25\%$ of the sampling clock phase in each THA for all frequency range. This means that each delay cell has to have a wide programmable delay range to meet the specification. In addition, the ADC test chip has to transmit all the samples *without decimation*, thus the complete information can be used on an off-chip processor.

B. Input Variable Gain Amplifier

The analog input signal of the chip is buffered with a digitally controlled variable-gain amplifier (VGA). This block is required to allow an automatic gain control (AGC) of the input signal for optimum dynamic range. The VGA has three active stages (Fig. 2) and each stage consists of 48 differential pairs connected in parallel with an offset cancellation loop [9]. The gain of the stages is $A_v \propto g_m$, where g_m is the MOS transconductance. Then, turning on/off each differential pair of each stage, the number of active MOS is changed then g_m (and A_v) can be controlled. The total current and load resistor of each stage of the VGA is kept constant, thus the output common-mode voltage does not change. Moreover, the analog input is first connected to a passive attenuator before connecting to VGA in order to reduce distortion. If the gain control is not required, the VGA can be bypassed with MOS switches therefore the VGA distortion can be avoided.

C. Time-Interleaved ADC

The core of the chip is a hierarchical interleaved ADC (see Fig. 1). It includes 8 parallel channels (slices) where each channel consists of one THA and two sub-interleaved SAR ADC. Each THA is managed by a 50% duty cycle clock at frequency $F_{slice} = F_s/8 = 2\ \text{GHz}/8 = 250\ \text{MHz}$. After tracking, the THA turns to the *hold* mode and the signal is re-sampled alternatively by one of the two SAR ADC for

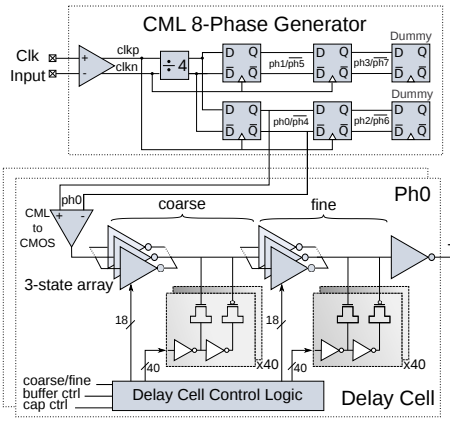

Fig. 3. 8-Phase generator and delay-cell blocks.

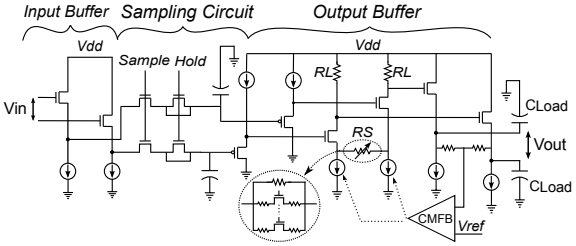

Fig. 4. THA with gain calibration stage.

quantization. The THA and SARs are synchronized by a clock divider that generates two clock signals from THA clock with 25% duty cycle at $F_{SAR} = F_{slice}/2 = 125\text{MHz}$. After the quantization, the two SAR outputs are multiplexed to provide a single 6 bits output at F_{slice} rate.

The eight THA clock phases are provided by a multiple-phase clock generator as depicted in Fig. 3. It is based on a double shift-register (SR) therefore an 1 GHz clock input is needed from an off-chip generator in order to achieve 2 GHz sampling rate. The shift registers are implemented in current-mode-logic (CML) to minimize the clock jitter coupled from power supply. Moreover, a CML clock divider is needed to provide the clock pattern at the SR input. In addition, the CML divider is optimized to operate on a wide range of input clock frequencies (100 MHz to 1 GHz) with maximum sensitivity [10].

Finally, the digital slice outputs (8 channels $\times$ 6 bits) are sent to the transmitter (TX). In the TX, the 48 digital slice outputs are multiplexed by 4 to arrange a 12 parallel LVDS channels interface. Note that, unlike most of reported Giga-sampled ADC test chips [4]–[6], in our design the full data rate (12 Giga-bits per second (Gbps)) without decimation is sent off-chip.

D. Track and Hold Amplifier

The THA topology is presented in Fig. 4. It is composed of an input buffer stage, a sampling circuit, and an output buffer. The input buffer is a pseudo-differential source follower that drives an NMOS sampling circuit. The input-buffer (plus sampling circuit) bandwidth (BW) is near 4 GHz. This over-bandwidth at the THA input buffer avoids BW mismatch at

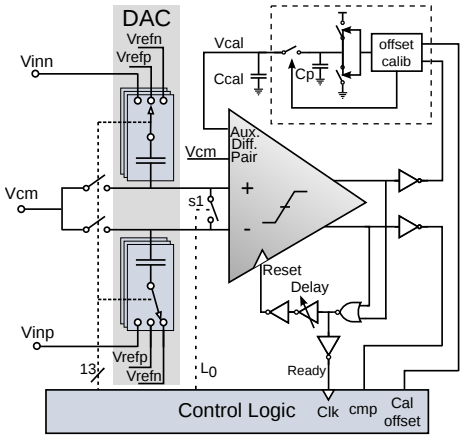

Fig. 5. Asynchronous SAR ADC topology.

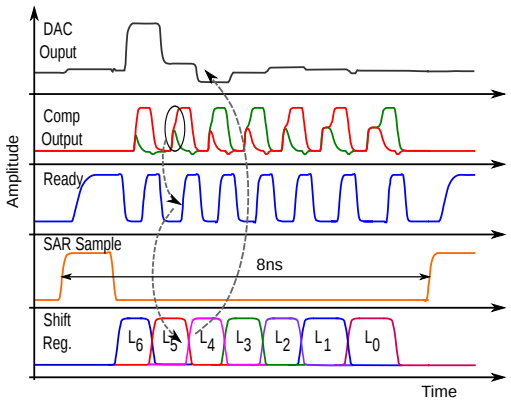

Fig. 6. Asynchronous SAR ADC timing diagram.

Nyquist input frequencies. Moreover, from simulations we verified that the linearity at the sampling circuit is above 60 dB. The output buffer is a 3 stage amplifier where a pseudo-differential common-source degeneration amplifier is used to calibrate the gain mismatch between THAs. The gain is controlled by R_L and R_S as $A_v = R_L/(1/g_m + R_S)$. The value of R_S is digitally programmed connecting in parallel a fixed resistor with one of the 16 branches of a resistor array.

On the other hand, a last stage source follower buffer is used to drive one of the two SAR digital-to-analog converters (DAC) that alternatively loads the THA. The source follower output stage allows a low SAR DAC settling time ($\tau < 150$ ps worst case corner) considering a C_L equivalent DAC capacitor array of 600 fF. Besides, the *total harmonic distortion* (THD) at the SAR inputs is -48 dB.

E. Programmable Delay Cell

The design of digitally programmable delay cells for TI-ADC phase calibration applications has been widely studied [4]–[6]. Figure 3 shows the delay cells circuit used between the phase generator and the THAs. These cells are able to set a time delay (T_d) to control the relative sampling time between the clock phases. This design considers a fine delay circuit and a coarse delay circuit. The fine delay circuit is used to adjust very small sampling time mismatch. The fine delay range is $T_{d_{max}} = \pm 0.03 T_s$ with 40 steps of $T_{d_{step}} = 0.0015 T_s$, where $T_s = 1/F_s$ is the overall sampling period.

As explained in Section II-A, a wide phase control is needed to emulate any relatively large sampling mismatch scenario (e.g., high-speed TI-ADC in optical receivers [8]). Therefore, a coarse delay circuit is implemented with a programmable range of $T_{d_{max}} = \pm 0.3 T_s$ and $T_{d_{step}} = 0.015 T_s$. The fine and coarse delay circuit are based on a shunt-capacitor technique where each buffer is loaded by a 40 equal sized MOS capacitor array (MOScap) that is thermometrically switched [6].

Moreover, the ADC can operate from 200 MS/s to 2 GS/s with T_s varying from 5 ns to 500 ps, respectively. Hence, the delay cell has to be able to vary $T_{d_{step}}$. The solution for the programmability of $T_{d_{step}}$ was the addition of a current control which comprises of 18 equal-sized 3-*state buffers* that allow for the variation of the charge/discharge current of the MOScap array. With the combination of both time delay techniques, the coarse $T_{d_{step}}$ can be set from 7.5 ps to 75 ps and the fine $T_{d_{step}}$ from 0.75 ps to 7.5 ps.

III. Asynchronous SAR ADC

The asynchronous SAR ADC topology is shown in Fig. 5. It is based on a binary-weighted redistribution-charge DAC, a latched comparator, and a self-clocked asynchronous control logic. The capacitor array is composed of metal-fringe capacitor unit-cells of 6.5 fF. The latched comparator used is a PMOS StrongArm [11] with a resistive load differential pre-amplifier. Moreover, the pre-amplifier has an auxiliary differential pair for offset calibration [12].

Figure 6 shows the asynchronous SAR timing diagram. The sequence starts with the *SAR sample* signal, provided by the internal slice divider and the SAR internal logic (see Fig. 1). Then, the shift-register (SR) is clocked and the DAC is set for MSB comparison. When the comparison ends, a detector (NOR gate at the comparator outputs) toggles the *ready signal* that is buffered to clock the SR. After that, the control logic sets the DAC and the comparator is reset to allow the next comparison cycle. Moreover, from the *critical timing path* of control logic, a carefully custom logic implementation is used to achieve high-speed and low power consumption in all the flip-flops and combinational gates.

A. Calibration of the Comparator Offset

The offset of the comparator defines the SAR offset (without considering the THA offset), and it can take large values (several LSBs) for small area comparators. Therefore, a comparator offset calibration is required to avoid intra-slice offset mismatch (i.e., between the two sub-interleaved SAR)[1] .

As shown in the timing diagram of Fig. 6, after the 6 bits comparison cycles, the signal L_0 closes the switch S_1 and the comparator inputs are shorted. Since no input voltage is applied, the next comparison will be decided as a result of the offset voltage at the latch regeneration nodes, including pre-amp and latch offset effects. As proposed in [12], the comparison result is stored as a fixed charge in a small (parasitic) capacitor C_p and then it is averaged with the past

[1]Note that each THA buffer introduces an inter-slice offset, but this mismatch is compensated with a digital off-chip processing.

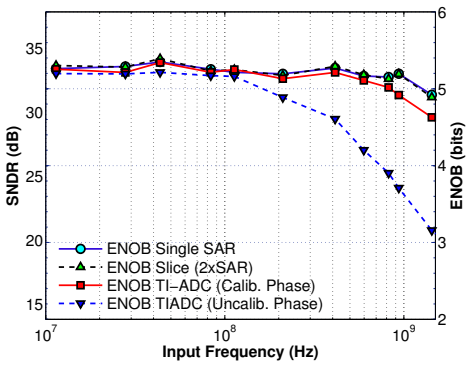

Fig. 7. SNDR and ENOB vs. input frequency.

decisions in an integration capacitor C_{cal}. Finally, the offset calibration loop is closed by the auxiliary differential pair on the pre-amplifier to compensate the equivalent input offset. Note that if there is a comparator metastable state (very long regeneration time) in the approximation cycle, this will not affect the quantization process. If it takes a long time, the offset calibration cycle will be skipped but it will not degrade the offset calibration. A similar scheme has been used recently in [13].

IV. Experimental Results

The TI-ADC was fabricated in a 0.13μm standard CMOS process and occupies a 1.8mm x 1.8mm area (without including Tx and VGA). In the following, some experimental results of the fabricated TI-ADC with a sampling rate of $F_s = 2\mathrm{GS/s}$ are presented[2].

Figure 7 shows the SNDR and the effective-number-of-bits (ENOB) as a function of the analog input frequency, F_{in}. The performance of a single SAR converter achieves a peak SNDR of 34.2 dB (5.39 ENOB) and 33 dB (5.2 ENOB) at near Nyquist input frequencies. Moreover, the slice channel shows less than 0.3 dB SNDR degradation compared to a single SAR in all the measured bandwidth. This means that the comparator offset calibration circuit works properly and no intra-slice offset mismatch is noted between the two sub-interleaved SAR ADC. Also, the TI-ADC achieves a peak SNDR of 33.9 dB (same as the slice) at low F_{in} after the off-chip compensation of the gain and offset of the THA. A predictable SNDR degradation can be noted at high input frequencies due to sampling phase mismatch. However, after the *manually* delay cells adjustment on each sampling phase, an SNDR of 31.4 dB (4.92 ENOB) is achieved for the complete TI-ADC at $F_s = 2\mathrm{GS/s}$.

For each SAR ADC, the power consumption is 3.3 mW at 1.2 V and the figure-of-merit defined as $FOM = Power/(2^{ENOB_{Nyq}} * F_s)$ is 0.63 (pJ/Conv-Step). The power consumption of the full TI-ADC is 192 mW (without considering VGA and Clock Phase Generator), while the overall FOM is 3.17(pJ/Conv-Step). The differential-non-linearity (DNL) and integral-non-linearity (INL) of the TI-ADC are 0.16 LSB and 0.49 LSB, respectively. Figure 8 shows the chip die micrograph.

[2]These measurements were done with the VGA bypassed.

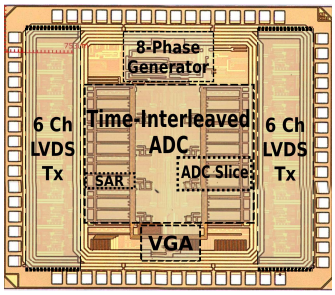

Fig. 8. Chip die photo. Die size: $3mm$ x $3.5mm$.

V. Conclusions

A 6-bit 2-GS/s TI-SAR ADC has been designed, fabricated, and characterized. The implemented TI-ADC provides an excellent platform to evaluate mixed-signal calibration techniques, which are of great interest for application in high-speed optical systems.

Acknowledgement

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